In the Claims:

1. (Original) An electrical fuse comprising:

a cathode doped with a first impurity of a first conductivity type;

an anode doped with a second impurity of a second conductivity type;

one or more links electrically coupling the cathode and the anode, each link having a first portion and a second portion, the first portion being doped with the first impurity, the second portion being doped with the second impurity, one or more p-n junction diodes being formed at a junction between the first portion and the second portion; and

a conductive layer over the p-n junction diodes.

2. (Original) The electrical fuse of claim 1, wherein the first impurity is a p-type impurity and the second impurity is an n-type impurity.

3. (Original) The electrical fuse of claim 1, wherein the conductive layer is a silicide.

4. (Original) The electrical fuse of claim 1, wherein the conductive layer is less than 500 Å in thickness.

5. (Original) The electrical fuse of claim 1, wherein the conductive layer is a material selected from the group consisting essentially of titanium silicide, cobalt silicide, nickel silicide, platinum silicide, and a combination thereof.

6. (Original) The electrical fuse of claim 1, wherein the cathode, the anode, and the links comprise polysilicon.

7. (Original) The electrical fuse of claim 1, wherein the cathode, the anode, and the links are less than 2500 Å in thickness.

8. (Original) The electrical fuse of claim 1, further comprising one or more contacts electrically coupled to the cathode and one or more contacts electrically coupled to the anode.

9. (Original) The electrical fuse of claim 1, further comprising a first contact array comprising a plurality of contacts electrically coupled to the cathode, and further comprising a second contact array comprising a plurality of contacts electrically coupled to the anode.

10. (Original) The electrical fuse of claim 1, wherein the cathode and the anode are symmetric.

11. (Original) A method of forming an electrical fuse, the method comprising:

forming a cathode, an anode, and one or more links interconnecting the cathode and the anode on a substrate, each link having a first portion and a second portion;

doping the anode with a first impurity;

doping the first portion with the first impurity;

doping the cathode with a second impurity;

doping the second portion with the second impurity; and

forming a conductive layer on the links over junctions between the first portion and the second portion.

12. (Original) The method of claim 11, wherein the first impurity is a p-type impurity and the second impurity is an n-type impurity.

13. (Original) The method of claim 11, wherein the conductive layer is a silicide.

14. (Original) The method of claim 11, wherein the conductive layer is less than 500 Å in thickness.

15. (Original) The method of claim 11, wherein the conductive layer is a material selected from the group consisting essentially of titanium silicide, cobalt silicide, nickel silicide, platinum silicide, and a combination thereof.

16. (Original) The method of claim 11, wherein the cathode, the anode, and the links comprise polysilicon.

17. (Original) The method of claim 11, wherein the cathode, the anode, and the links are less than 2500 Å in thickness.

18. (Original) The method of claim 11, further comprising one or more contacts electrically coupled to the cathode and one or more contacts electrically coupled to the anode.

19. (Original) The method of claim 11, further comprising a first contact array comprising a plurality of contacts electrically coupled to the cathode, and further comprising a second contact array comprising a plurality of contacts electrically coupled to the anode.

20. (Original) The method of claim 11, wherein the cathode and the anode are symmetric.

In the Drawings:

The attached sheet of drawings replaces Figures 6 and 7. The modifications to Figures 6 and 7 include: changing element 614 to be an NMOS device rather than a PMOS device; modifying the reference V_{cc} to V_{ss} on the left side of Figures 6 and 7, and inserting V_{cc} on the right side of Figures 6 and 7.